Quad ISDN 4B3T Echocanceller Digital Frontend DFE-T

PEB 24901 Versions 1.1/1.2

Addendum/Corrections 07.99 to the prel. Data Sheet 02.95 (Version 1.1) and to the Delta Sheet 06.96 (Version 1.2)

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1 Electrical Characteristics

Testconditions:

VDD = 4.75 to 5.25 V

Ambient temperature under bias:
PEB 24901 0 to 70 °C
PEF 24901 – 40 to 85 °C

1.1 Static Characteristics

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
High-level input voltage	V_{IH}	2.0	V_{DD} + 0.3	V	
Low-level input voltage	V_{IL}		0.8	V	
Low-level input leakage current	I_{IL}	-1		µA	V_I = GND
High-level input leakage current	I_{IH}		1	µA	V_I = VDD
Low-level leakage current pull up pins	I_{IT}	-500		µA	V_I = GND
High-level output voltage (except DOUT, relay driver pins D0A .. D3D)	V_{OH1}	2.4		V	I_{OH1} = 0.4 mA

Revision History: Previous Version:
Major Changes:

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
High-level output voltage for DOUT	V_{OH2}	3.5		V	IOH2 = –6 mA
High-level output voltage for relay driver pins D0A .. D3D	V_{OH3}	2.4		V	IOH3 = –2 mA
Low-level output voltage	V_{OL1}		0.4	V	IOL1 = 2 mA
Low-level output voltage for DOUT	V_{OL2}		0.5	V	IOL1 = 7 mA
Input capacitance	C_{IN}		10	pF	

Note: Inputs at VDD/GND

1.2 Dynamic Characteristics

Ambient temperature under bias range, V_{DD} = 5 V ± 5 %.

Inputs are driven to 2.4 V for a logical ’1’ and to 0.4 V for a logical ’0’.
Timing measurements are made at 2.0 V for a logical ’1’ and at 0.8 V for a logical ’0’.
The AC-testing input/output wave forms are shown below. The test load is 100pF, unless otherwise indicated.

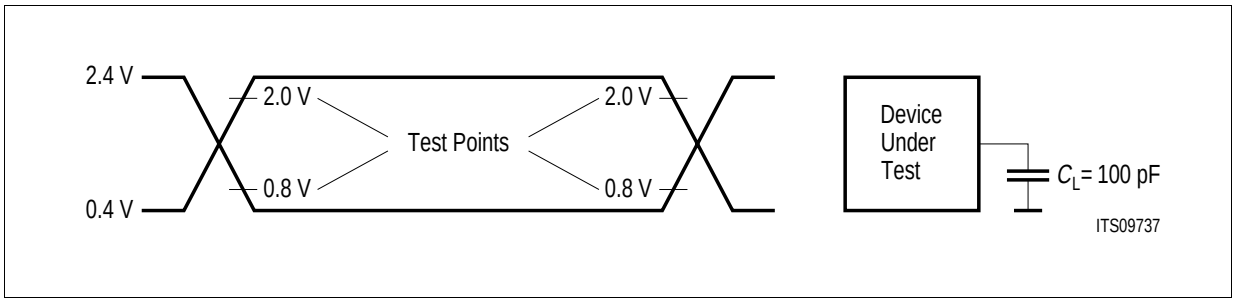

Figure 1 I/O-Wave Form for AC-Test

IOM-2 Timing

In case the period of signals is stated the time reference will be at 1.4 V; in all other cases 0.8 V (low) and 2.0 V (high) thresholds are used as reference.

The dynamic characteristics of the IOM-2-interface is given in **figure 2**.

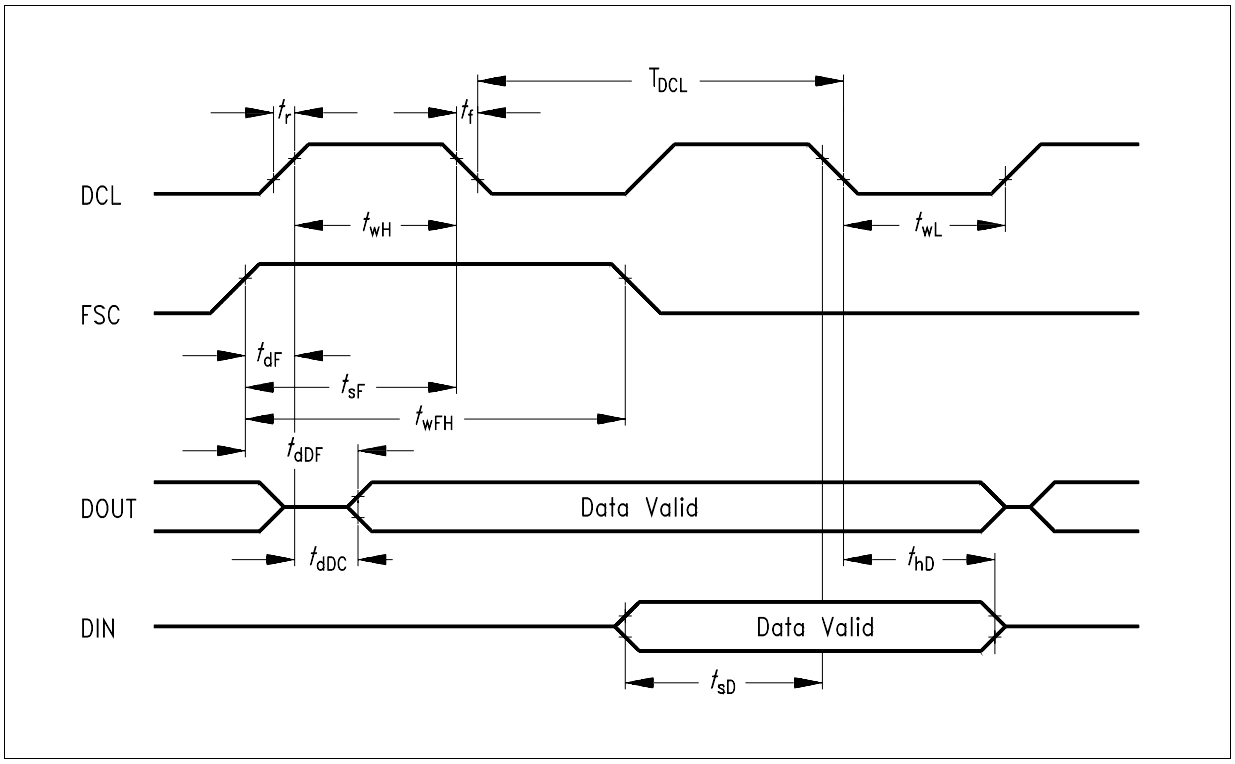

Figure 2 IOM®-2 Timing of IOM-2 Interface (Detail)

Table 1 IOM®-2 Dynamic Input Characteristics

Parameter	Signal	Symbol	Limit Values		Unit
			min.	max.	
Data clock rise/fall	DCL	t_r, t_f		60	ns
Clock period		T_{DCL}	122		ns
Pulse width high/low		t_{wH} t_{wL}	53 53		ns ns
Frame synch. rise/fall	FSC	t_r, t_f		60	ns
Frame setup		t_{sF}	30		ns
Frame hold		t_{dF}		t_{wL} – 30	ns
Frame width high/low [1)]		t_{wFH} t_{wFL}	100 $2 \times T_{DCL}$		ns
Data setup	DIN	t_{sD}	t_{wH} + 20		ns
Data hold		t_{hD}	50		ns

Note: This is in accordance with the IOM-timing specification. For correct functional operation the high period must be 1×T_{DCL} for superframe markers and at least 2×T_{DCL} for non-superframe markers.

Table 2 IOM®-2 Dynamic Output Characteristics

Parameter	Signal	Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Data delay/clock [1]	DOUT	t_{dDC}			100	ns	C_L = 150 pF
Data delay/frame [1]	DOUT	t_{dDF}			150	ns	C_L = 150 pF

Note: The point of time at which the output data will be valid is referred to the rising edges of either FSC (t_{dDF}) or DCL (t_{dDC}). The rising edge of the signal appearing last (normally DCL) shall be the reference.

Boundary Scan Timing

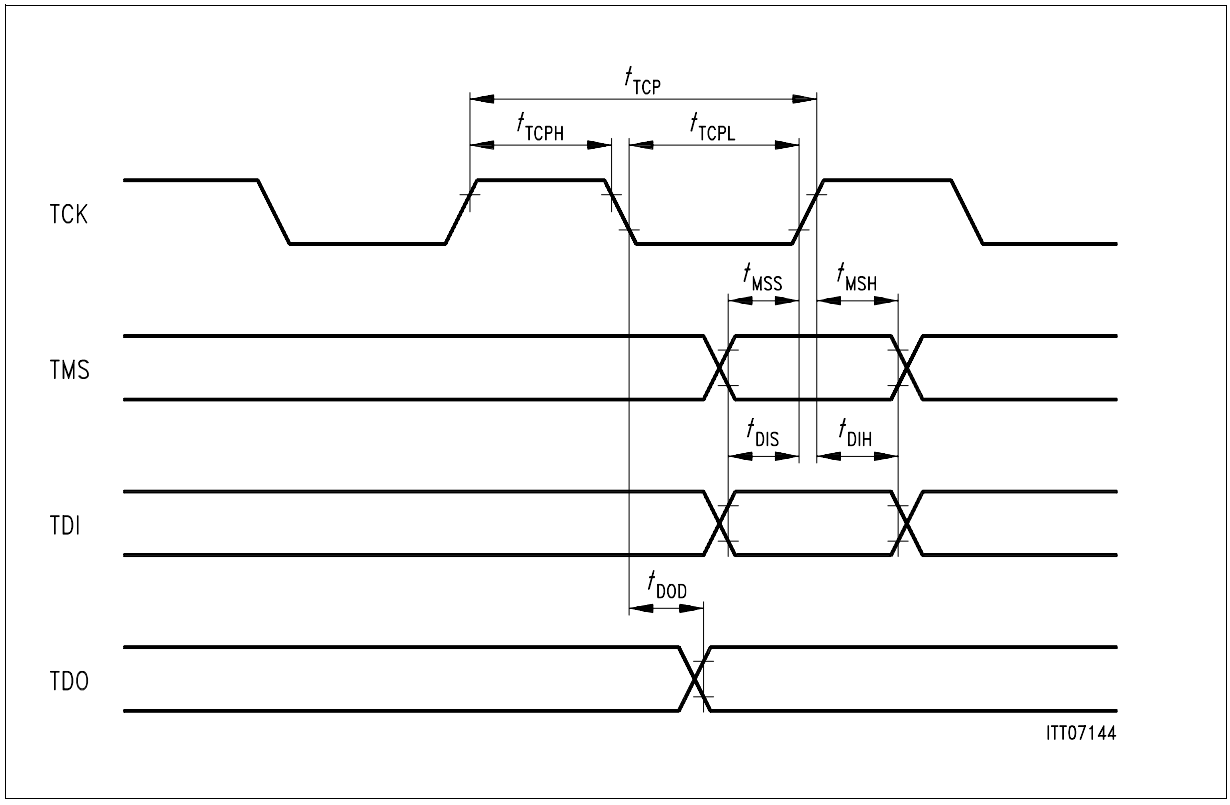

Figure 3 Boundary Scan Timing

Table 3 Boundary Scan Dynamic Timing Requirements

Parameter	Symbol	Limit Values		Unit
		min.	max.	
test clock period	t_{TCP}	160	-	ns
test clock period low	t_{TCPL}	70	-	ns
test clock period high	t_{TCPH}	70	-	ns
TMS set-up time to TCK	t_{MSS}	30	-	ns
TMS hold time from TCK	t_{MSH}	30	-	ns
TDI set-up time to TCK	t_{DIS}	30	-	ns
TDI hold time from TCK	t_{DIH}	30	-	ns
TDO valid delay from TCK	t_{DOD}	-	60	ns

Interface to the Quad IEC AFE

The AC characteristics of the AFE-interface pins are optimized to fit to AFE Versions 1.1/ 1.2/2.1 if the following loads are no exceeded. It is required, that both devices are supplied by the same 5 Volt source (VDD) .

Table 4 Interface Signals of AFE and DFE-T

Pin	Signal Driving Device	Max. Capacitve load
CL15	AFE	50 pF
SDR	AFE	20 pF
PDM1..4	AFE	20 pF
SDX	DFE-T	20 pF

1.3 Power Supply

Supply voltages

V_{DD}= + 5 V ± 0.25 V

Power Consumption

All measurements with random 2B + D data in active states.

Mode	Test conditions	Typ. values	Max. values	Unit
Power-up all Channels ?	5.00 V, open outputs, inputs at V_{DD} /V_{SS}	50	70	mA
Power-down	5.00 V, open outputs, inputs at V_{DD} /V_{SS}	15	25	mA

1.4 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias: PEB PEF	T_A	 0 to 70 – 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Supply voltage	V_{DD}	– 0.3 < V_{DD} < 7.0	V
Input voltage	V_I	– 0.3 < V_I < V_{DD} + 0.3 (max. 7)	V
Output voltage	V_O	– 0.3 < V_O < V_{DD} + 0.3 (max 7)	V
Max. voltage between different GND pins	V_S	± 250	mV
Max. voltage between different VDD pins	V_S	± 250	mV
Storage temperature	T_{stg}	– 65 to 125	°C
Ambient temperature PEB 24901 PEF 24911	 T_A T_A	 0 to 70 – 40 to 85	 °C °C
Thermal resistance (system-air) (system-case)	 $R_{th\ SA}$ $R_{th\ SC}$	 55 15	 K/W K/W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may affect device reliability. This is a stress rating only and functional operation of the device under those conditions or at any other condition beyond those indicated in the operational conditions of this specification is not implied. It is not implied, that more than one of those conditions can be applied simultaneously.