**Table 9: DC Parameters** (Die)

| Symbol | Parameters | Min(2) | Typ(1) | Max(2) | Units | Conditions |
|---|---|---|---|---|---|---|
| $A_{ARP}$ | ANA IN to SP+/- Gain | | 22 | | dB | |
| $R_{AGC}$ | AGC Output Resistance | | 5 | | KΩ | |
| $I_{PREH}$ | Preamp Out Source | | –2 | | mA | @ $V_{OUT}$ = 1.0 V |
| $I_{PREL}$ | Preamp In Sink | | 0.5 | | mA | @ $V_{OUT}$ = 2.0 V |

1. *Typical values @ $T_A$ = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *$V_{CCA}$ and $V_{CCD}$ connected together.*
4. *$\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$ must be at $V_{CCD}$.*
5. *$\overline{REC}$, $\overline{PLAYL}$, and $\overline{PLAYE}$, A6, A7.*
6. *A0–A5, XCLK.*

**Table 10: AC Parameters** (Die)

| Symbol | Characteristic | | Min(2) | Typ(1) | Max(2) | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $F_S$ | Sampling Frequency | ISD1110<br>ISD1112 | | | 6.4<br>5.3 | KHz<br>KHz | (5)<br>(5) |
| $F_{CF}$ | Filter Pass Band | ISD1110<br>ISD1112 | | 2.6<br>2.2 | | KHz<br>KHz | 3 dB Roll-Off Point(3)(6)<br>3 dB Roll-Off Point(3)(6) |
| $T_{REC}$ | Record Duration | ISD1110<br>ISD1112 | 10<br>12 | | | sec<br>sec | |
| $T_{PLAY}$ | Playback Duration | ISD1110<br>ISD1112 | 10<br>12 | | | sec<br>sec | (5)<br>(5) |
| $T_{LED1}$ | $\overline{RECLED}$ ON Delay | | | 5 | | µsec | |
| $T_{LED2}$ | $\overline{RECLED}$ OFF Delay | ISD1110<br>ISD1112 | 40<br>50 | 48.5<br>58.3 | 100<br>105 | msec<br>msec | |
| $T_{SET}$ | A0–A7 Setup Time | | 300 | | | nsec | |
| $T_{HOLD}$ | A0–A7 Hold Time | | 0 | | | nsec | |
| $T_{RPUD}$ | Record Power-Up Delay | ISD1110<br>ISD1112 | | 32<br>39 | | msec<br>msec | |
| $T_{RPDD}$ | Record Power-Down Delay | ISD1110<br>ISD1112 | | 32<br>39 | | msec<br>msec | |
| $T_{PPUD}$ | Play Power-Up Delay | ISD1110<br>ISD1112 | | 32<br>39 | | msec<br>msec | |
| $T_{PPDD}$ | Play Power-Down Delay | ISD1110<br>ISD1112 | | 8.1<br>9.7 | | msec<br>msec | |

**Table 10: AC Parameters** (Die)

| Symbol | Characteristic | | Min[2] | Typ[1] | Max[2] | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $T_{EOM}$ | EOM Pulse Width | ISD1110<br>ISD1112 | | 15.625<br>18.75 | | msec<br>msec | |
| THD | Total Harmonic Distortion | | | 1 | | % | @ 1 KHz |
| $P_{OUT}$ | Speaker Output Power | | | 12.2 | | mW | $R_{EXT}$ = 16 Ω |
| $V_{OUT}$ | Voltage Across Speaker Pins | | | 1.25 | 2.5 | mVp–p | $R_{EXT}$ = 600 Ω |
| $V_{IN1}$ | MIC Input Voltage | | | | 20 | mV | Peak-to-Peak[4] |
| $V_{IN2}$ | ANA IN Input Voltage | | | | 50 | mV | Peak-to-Peak |

1. *Typical values @ $T_A$ = 25°C and 5.0 V.*
2. *All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).*
4. *With 5.1 KΩ series resistor at ANA IN.*
5. *Sampling frequency and playback duration will vary as much as ±2.25 percent over the commercial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Filter specification applies to the antialiasing filter and to the smoothing filter.*

## TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (DIE)

**Chart 5: Record Mode Operating Current ($I_{CC}$)**

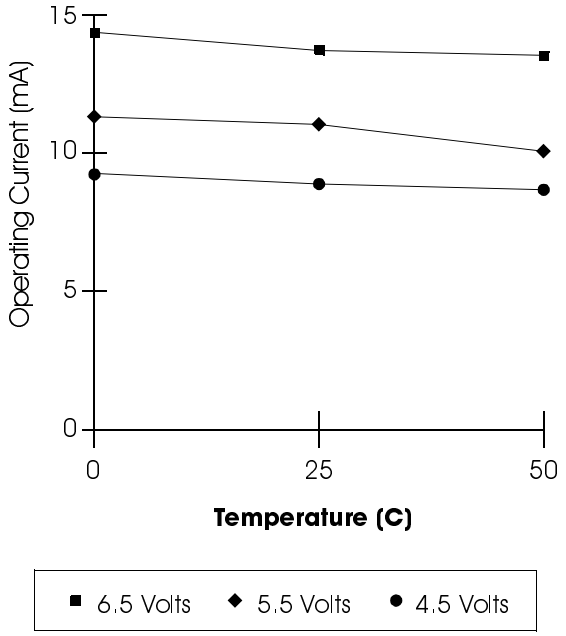



**Chart 6: Total Harmonic Distortion**

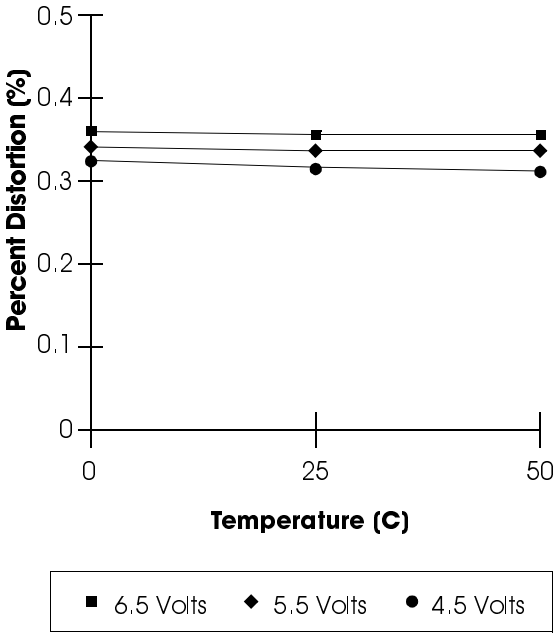



**Chart 7: Standby Current ($I_{SB}$)**

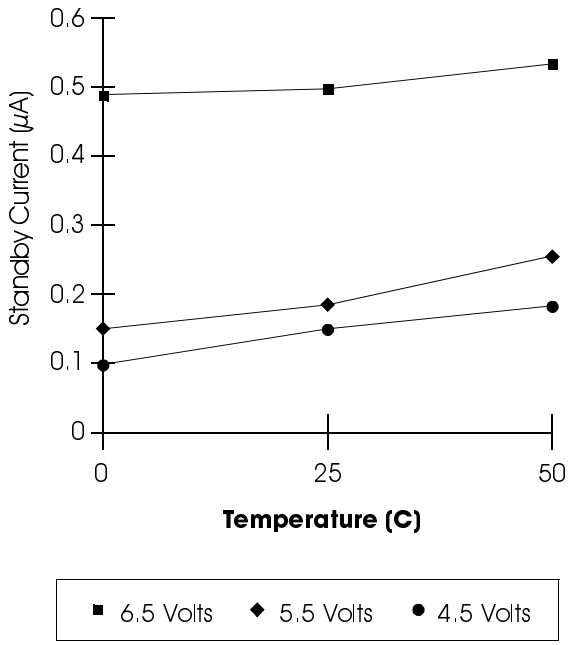



**Chart 8: Oscillator Stability**

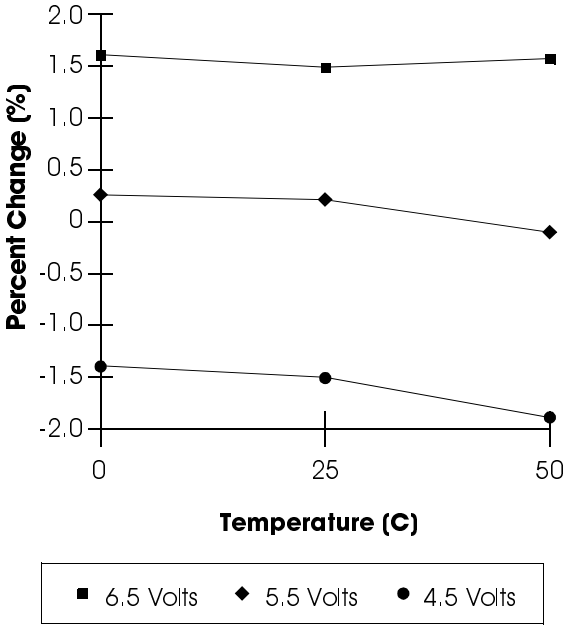
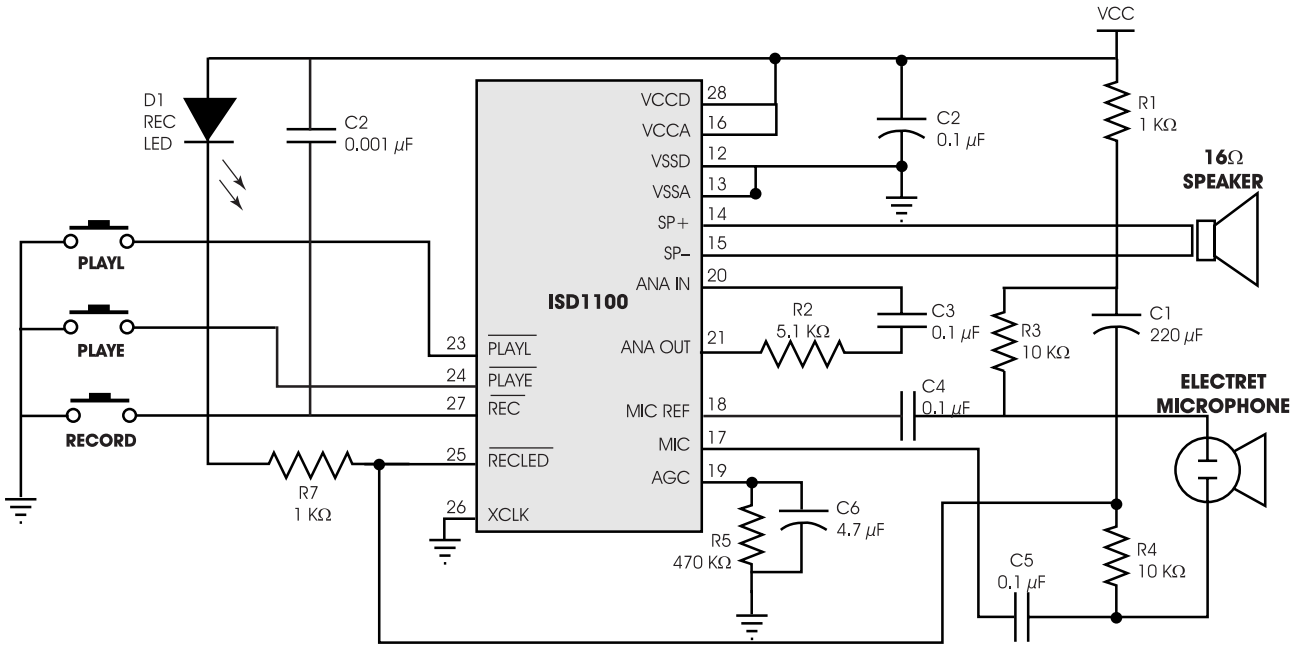


**Figure 4: Application Example**




## FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequence demonstrates the functionality of the ISD1100 series devices.

1. Record a message filling the memory.

   Pulling the $\overline{\text{REC}}$ signal LOW initiates a record cycle from the beginning of the message space. If $\overline{\text{REC}}$ is held LOW, the recording continues until the message space has been filled. Once the message space is filled, recording ceases. The device will automatically power down after $\overline{\text{REC}}$ is released HIGH. An EOM marker is written at the end of memory.

2. Edge-activated playback.

   Pulling the $\overline{\text{PLAYE}}$ signal LOW initiates a playback cycle from the beginning of the message space. The rising edge of $\overline{\text{PLAYE}}$ has no effect on operation. If a recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYE}}$ initiates a new play cycle from the beginning of the memory.

3. Level-activated playback.

   Pulling the $\overline{\text{PLAYL}}$ signal LOW initiates a playback cycle from the beginning of the message space. If recording has filled the message space, the entire message is played. When the device reaches the EOM marker, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYL}}$ initiates a new play cycle from the starting address.

4. Level-activated playback (truncated).

   If $\overline{\text{PLAYL}}$ is pulled HIGH any time during the playback cycle, the device stops playing and enters the power-down mode. A subsequent falling edge on $\overline{\text{PLAYL}}$ initiates a new play cycle from the beginning of memory.

5. Record (interrupting playback).

   The $\overline{REC}$ signal takes precedence over other operations. Any LOW-going transition on $\overline{REC}$ initiates a new record operation from the beginning of the memory, regardless of any current operation in progress.

6. Record a message, partially filling the memory.

   A record operation need not fill the entire memory. Releasing the $\overline{REC}$ signal HIGH before filling the message space causes the recording to stop and an EOM marker to be placed. The device powers down automatically.

7. Play back a message that partially fills the memory.

   Pulling the $\overline{PLAYE}$ or $\overline{PLAYL}$ signal LOW initiates a playback cycle which is then completed when the EOM marker is encountered. Playback ceases and the device powers down.

8. $\overline{RECLED}$ operation.

   The $\overline{RECLED}$ output pin provides an active-LOW signal which can be used to drive an LED as a "record-in- progress" indicator. It returns to a HIGH state when the $\overline{REC}$ pin is released HIGH or when the recording is completed due to the memory being filled. This pin also pulses LOW to indicate an EOM at the end of a message being played.

## APPLICATIONS NOTE

Some users may experience an unexpected recording taking place when their circuit is powered up, or the batteries are changed, and $V_{CC}$ rises faster than $\overline{REC}$. This undesired recording prevents playback of the previously recorded message. A spurious EOM marker may appear at the very beginning of the memory, preventing access to the original message, and nothing is played.

To prevent this occurrence, place a capacitor (approximately. 0.001 $\mu$F) between the control pin, $\overline{REC}$, and $V_{CC}$. This pulls the control pin voltage up with $V_{CC}$ as it rises. Once the voltage is HIGH, the pull-up device will keep the pin HIGH until intentionally pulled LOW, preventing the false EOM marker.

Since this condition is dependent upon factors such as the capacitance of the user's printed circuit board, not all circuit designs will exhibit the spurious marker. It is recommended, however, that the capacitor is included for design reliability. A more detailed explanation and resolution of this occurrence is described in Application Information.

# ISD1100 SERIES PHYSICAL DIMENSIONS

**Figure 5: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)**

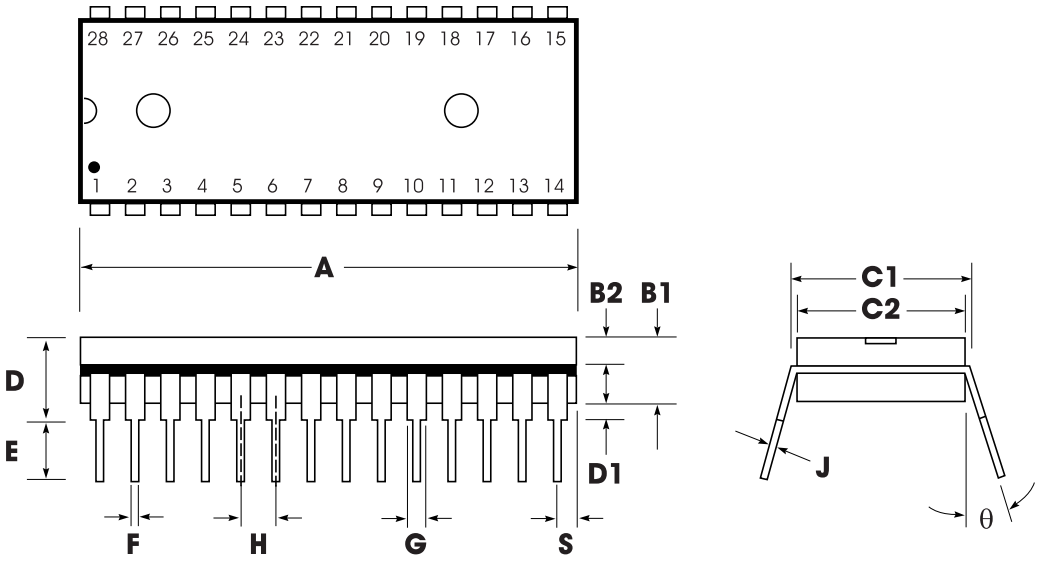



**Table 11: Plastic Dual Inline Package (PDIP) (P) Dimensions**

| | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 1.445 | 1.450 | 1.455 | 36.70 | 36.83 | 36.96 |
| B1 | | 0.150 | | | 3.81 | |
| B2 | 0.065 | 0.070 | 0.075 | 1.65 | 1.78 | 1.91 |
| C1 | 0.600 | | 0.625 | 15.24 | | 15.88 |
| C2 | 0.530 | 0.540 | 0.550 | 13.46 | 13.72 | 13.97 |
| D | | | 0.19 | | | 4.83 |
| D1 | 0.015 | | | 0.38 | | |
| E | 0.125 | | 0.135 | 3.18 | | 3.43 |
| F | 0.015 | 0.018 | 0.022 | 0.38 | 0.46 | 0.56 |
| G | 0.055 | 0.060 | 0.065 | 1.40 | 1.52 | 1.65 |
| H | | 0.100 | | | 2.54 | |
| J | 0.008 | 0.010 | 0.012 | 0.20 | 0.25 | 0.30 |
| S | 0.070 | 0.075 | 0.080 | 1.78 | 1.91 | 2.03 |
| q | 0° | | 15° | 0° | | 15° |

***NOTE:*** *Lead coplanarity to be within 0.005 inches.*

**Figure 6: 28-Lead 0.300-Inch Plastic Small OutLine Integrated Circuit (SOIC) (S)**

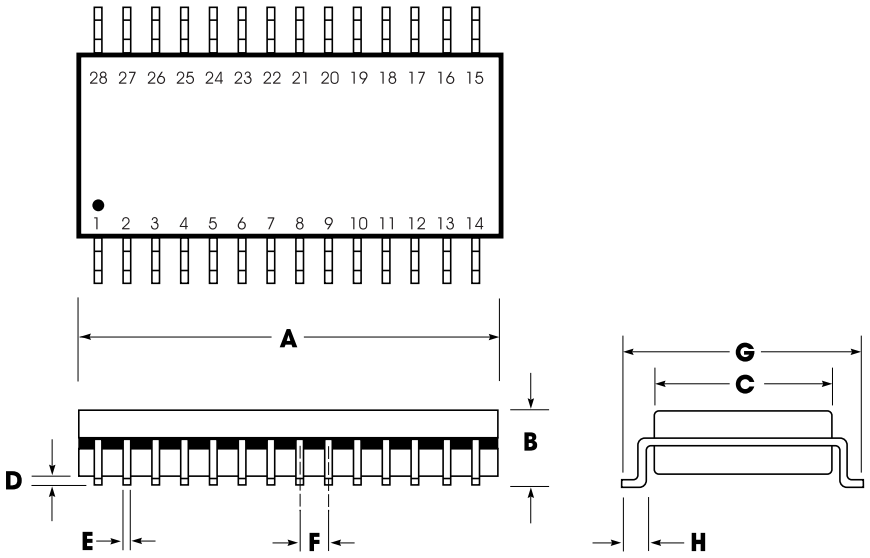



**Table 12: Plastic Small OutLine Integrated Circuit (SOIC) (S) Dimensions**

| | INCHES | | | MILLIMETERSþ | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.701 | 0.706 | 0.711 | 17.81 | 17.93 | 18.06 |
| B | 0.097 | 0.101 | 0.104 | 2.46 | 2.56 | 2.64 |
| C | 0.292 | 0.296 | 0.299 | 7.42 | 7.52 | 7.59 |
| D | 0.005 | 0.009 | 0.0115 | 0.127 | 0.22 | 0.29 |
| E | 0.014 | 0.016 | 0.019 | 0.35 | 0.41 | 0.48 |
| F | | 0.050 | | | 1.27 | |
| G | 0.400 | 0.406 | 0.410 | 10.16 | 10.31 | 10.41 |
| H | 0.024 | 0.032 | 0.040 | 0.61 | 0.81 | 1.02 |

***NOTE:*** *Lead coplanarity to be within 0.004 inches.*

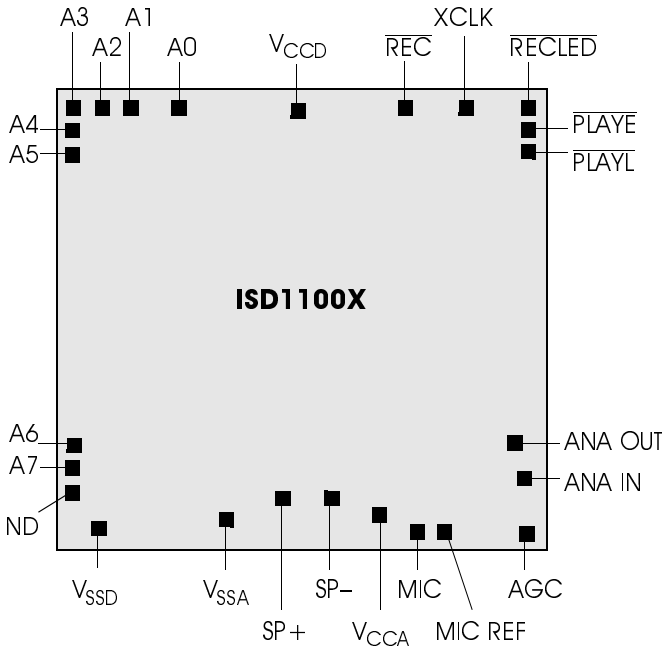
## Figure 7: ISD1100 Series Bonding Physical Layout[1]

ISD1100X

**I.** Die Dimensions
X: 172.2 ±1 mils
Y: 138.2 ±1 mils

**I.** Die Thickness(2)
17.5 ±1 mils

**I.** Pad Opening
88 x 112 microns
3.46 x 4.41 mils



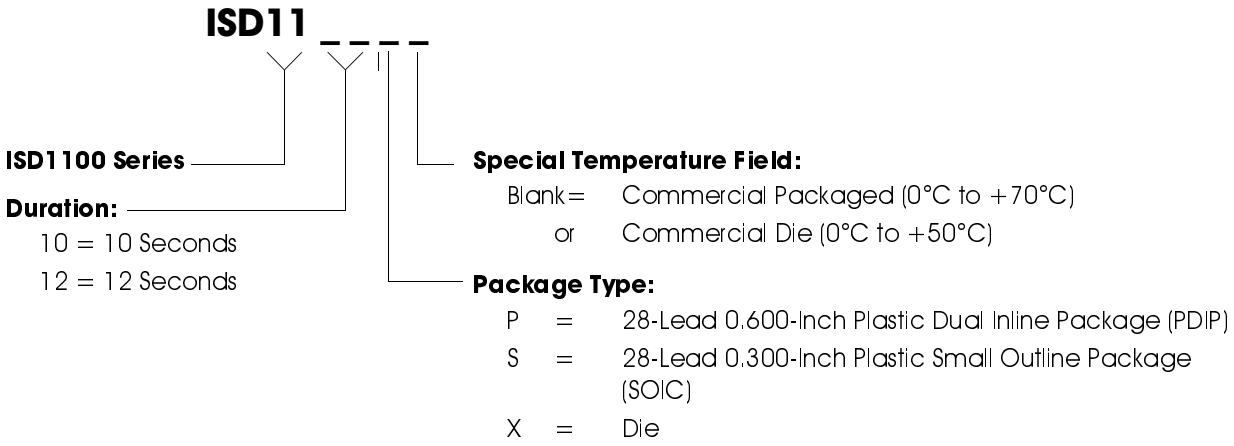

1. *The backside of die is internally connected to $V_{SS}$. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Die thickness is subject to change, please contact ISD factory for status.*

**Table 13: ISD1100 Series PIN/PAD Designations, with Respect to Die Center (µm)**

| Pin | Pin Name | X Axis | Y Axis |
|---|---|---|---|
| A0 | Address 0 | –1364.0 | 1589.6 |
| A1 | Address 1 | –1648.4 | 1589.6 |
| A2 | Address 2 | –1816.4 | 1589.6 |
| A3 | Address 3 | –2013.6 | 1515.6 |
| A4 | Address 4 | –2013.6 | 1337.6 |
| A5 | Address 5 | –2013.6 | 1129.6 |
| A6 | Address 6 | –2013.6 | –831.2 |
| A7 | Address 7 | –2013.6 | –1022.0 |
| NC | No Connect | –2013.6 | –1361.6 |
| $V_{SSD}$ | $V_{SS}$ Digital Power Supply | –1893.6 | –1588.0 |
| $V_{SSA}$ | $V_{SS}$ Analog Power Supply | –357.6 | –1588.0 |
| SP+ | Speaker Output + | –17.2 | –1512.8 |
| SP– | Speaker Output – | 412.4 | –1512.8 |
| $V_{CCA}$ | $V_{CC}$ Analog Power Supply | 780.0 | –1552.4 |
| MIC | Microphone Input | 992.0 | –1590.0 |
| MIC REF | Microphone Reference | 1169.2 | –1590.0 |
| AGC | Automatic Gain Control | 1978.4 | –1590.0 |
| ANA IN | Analog Input | 2005.6 | –1196.4 |
| ANA OUT | Analog Output | 1991.2 | –995.2 |
| $\overline{\text{PLAYL}}$ | Level-Activated Playback | 2014.4 | 1224.4 |
| $\overline{\text{PLAYE}}$ | Edge-Activated Playback | 2014.4 | 1392.8 |
| $\overline{\text{RECLED}}$ | Record LED Output | 2012.4 | 1587.6 |
| XCLK | No Connect (optional) | 1581.2 | 1589.6 |
| $\overline{\text{REC}}$ | Record | 752.8 | 1589.6 |
| $V_{CCD}$ | $V_{CC}$ Digital Power Supply | –48.0 | 1545.2 |

# ORDERING INFORMATION

### *Product Number Descriptor Key*




When ordering ISD1100 series devices, please refer to the following valid part numbers.

| Part Number | Part Number |
|---|---|
| ISD1110P | ISD1112P |
| ISD1110X | ISD1112X |
| ISD1110S | ISD1112S |

For the latest product information, access ISD's worldwide website at http://www.isd.com.