



## **Recommended Circuits and PCB Layout Considerations for IrMC Transceivers**

## ZHX1201/1203/1403/3403

The ZHX1201/1203/1403/3403 transceivers require layout considerations to maximize performance and to eliminate potential inductance problems. In mobile telephone layout, either single and separate voltage supplies are used. In applications where the distance from the supply voltage source to the IrDA module exceeds nine or ten inches, typical line inductance will be in the order of 300 to 400  $\mu$ H. With an optimum line matching resistor (see tables in Figure 1 and Figure 2), line inductance effects are minimized; further, the inclusion of this *vitaly important resistor*, together with the decoupling capacitor provides superior supply line decoupling as demonstrated by Graphs 1 and 2. Many IrDA-compliant transceivers, when operating with the above recommended component mix, yield improved throughput and a virtual absence of “re-tries.”

For small units, PDAs and so on, line lengths are shorter; therefore, a 51-ohm decoupling resistor together with a 1- $\mu$ F ceramic capacitor between V<sub>CC</sub> and ground, provide the necessary power supply decoupling for all data rates.

ZHX1201/1203/1403/3403 transceivers incorporate a current source that eliminates the need for an external resistor and makes a separate power supply unnecessary. However, if desired, a separate power supply can still be used.

For the ZHX1203/1403/3403 transceivers operating from a single supply, V<sub>CC</sub> must use a regulated supply between 2.1 and 3.6 volts (2.1 volts is the minimum V<sub>LED</sub> acceptable; will slightly reduce transmit range). If separate power supplies are used, V<sub>LED</sub> (voltage applied to the LEDA Pin) can be unregulated between 2.1 and 4.2 volts. See Figure 1 for the recommended schematic.

For the ZHX1201 using a single supply, V<sub>CC</sub> must use a regulated supply between 2.4 and 3.6 volts (2.4 volts is the minimum V<sub>LED</sub> acceptable). If separate power supplies are used, V<sub>LED</sub> (voltage applied to the LEDA Pin) may be unregulated between 2.4 and 4.2 volts. See Figure 2 for the recommended schematic

The inputs (Tx<sub>D</sub> and SD) and the output (Rx<sub>D</sub>) should be directly (DC) coupled to the I/O circuit. Capacitive coupling is unnecessary and must be avoided because the ZHX1201/1203/1403/3403 will automatically switch off the LED if the Tx<sub>D</sub> is accidentally kept active longer than approximately 180  $\mu$ s.

### Notes:

1. The shield tab must be soldered to ground, in one place only, for these devices to work properly. This avoids the formation of loop antennas.
2. The CMOS inputs TXD & SD. Logic to drive both these inputs must be low impedance and be either low (near GND) or high (near VCC).
3. If the device is driven by a tri-state source, or if the device pins experience high interference levels, it is recommended that 100K pull down resistors be used on either or both the TXD and SD pins.

## Application Block Diagrams-ZHXxx03

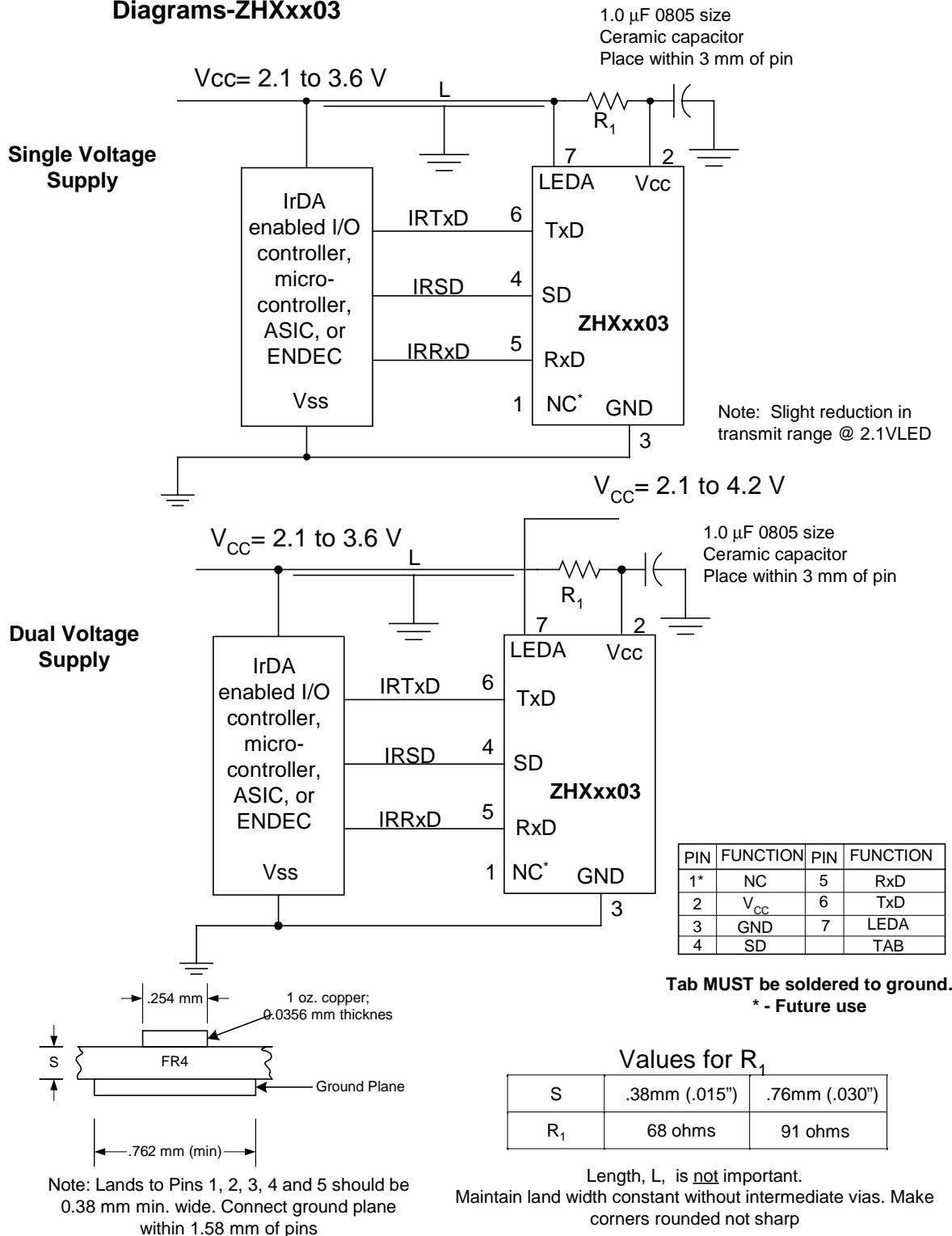


Figure 1. ZHX1203/1403/3403 Application Block Diagrams

### Application Block Diagrams-ZHX1201

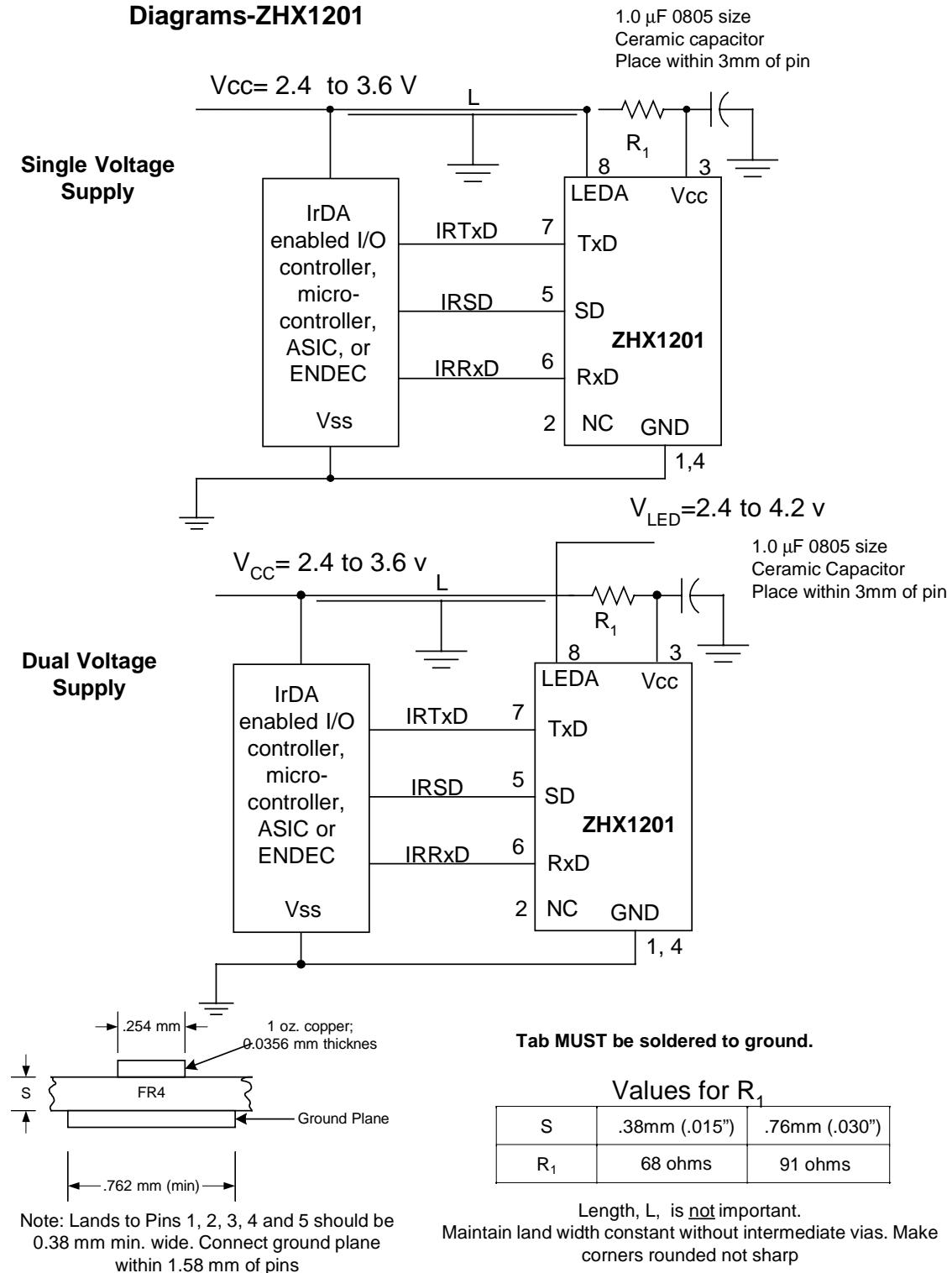


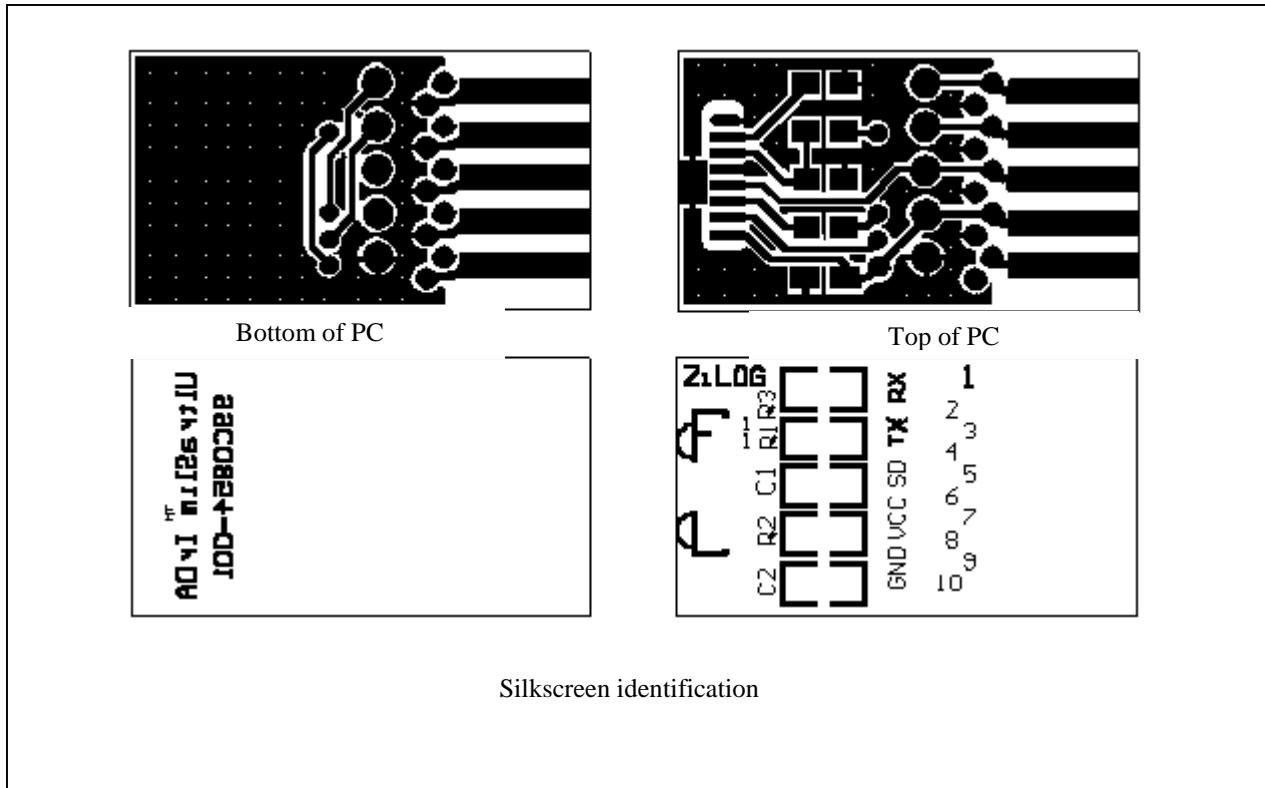
Figure 2. ZHX1201 Application Block Diagrams

## Shutdown

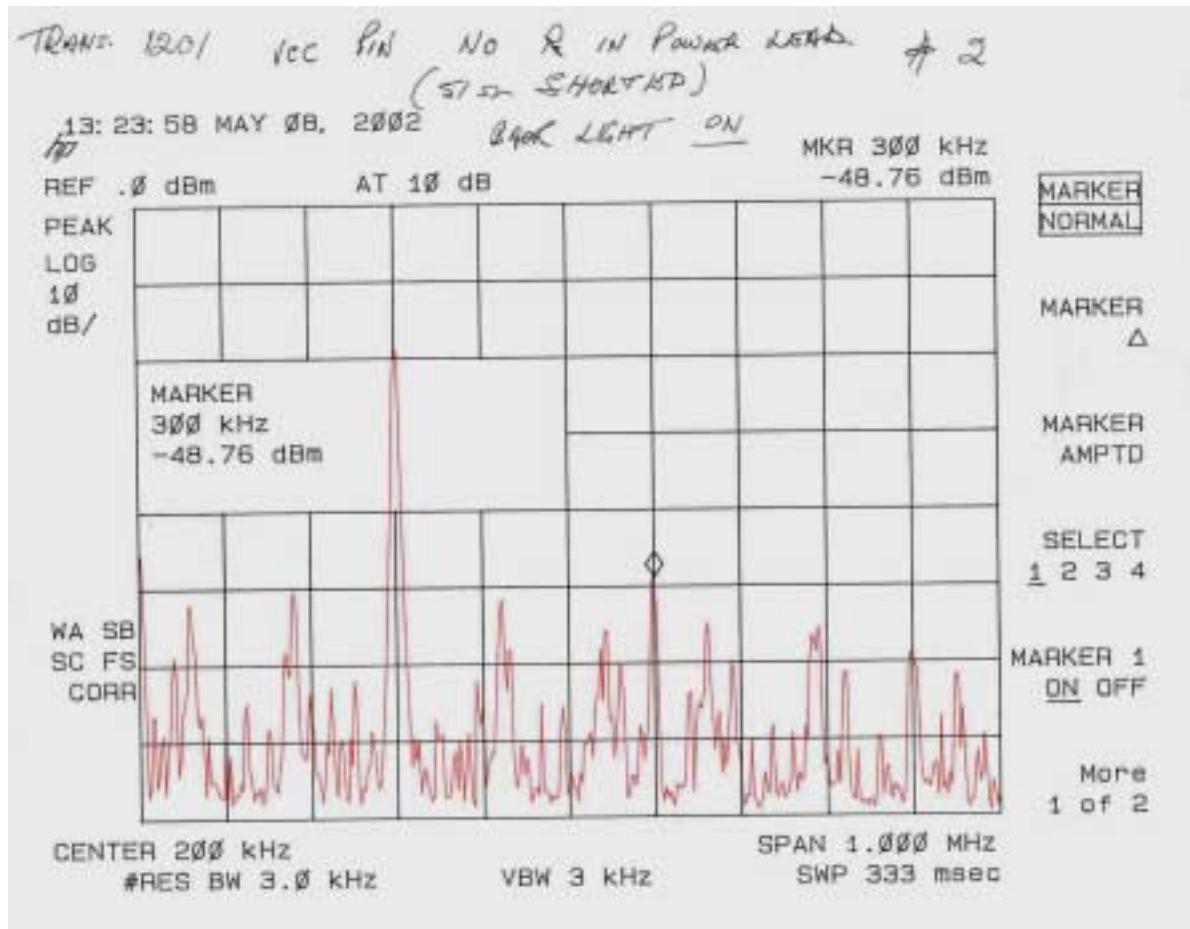
The ZHX1201/1203/1403/3403 can be very efficiently shut down while keeping the IRED connected to the power supply by enabling SD. LEDA can be maintained as an unregulated power supply. V<sub>CC</sub> can also remain connected to the regulated power supply. The voltage is limited at LEDA to 4.2 V and at V<sub>CC</sub> to 3.6 V. The recovery time from shut down to full sensitivity is less than 500 µs.

## Board Layout

Board layout is a key aspect of the overall design. While ZiLOG transceivers are designed to minimize problems, care must be taken when laying out the PCB particularly in high RF environments such as mobile telephones. Thin- or long-resistive and inductive wiring and traces must be avoided. ZiLOG can provide Gerber plots and samples of the described boards. See the following layouts.

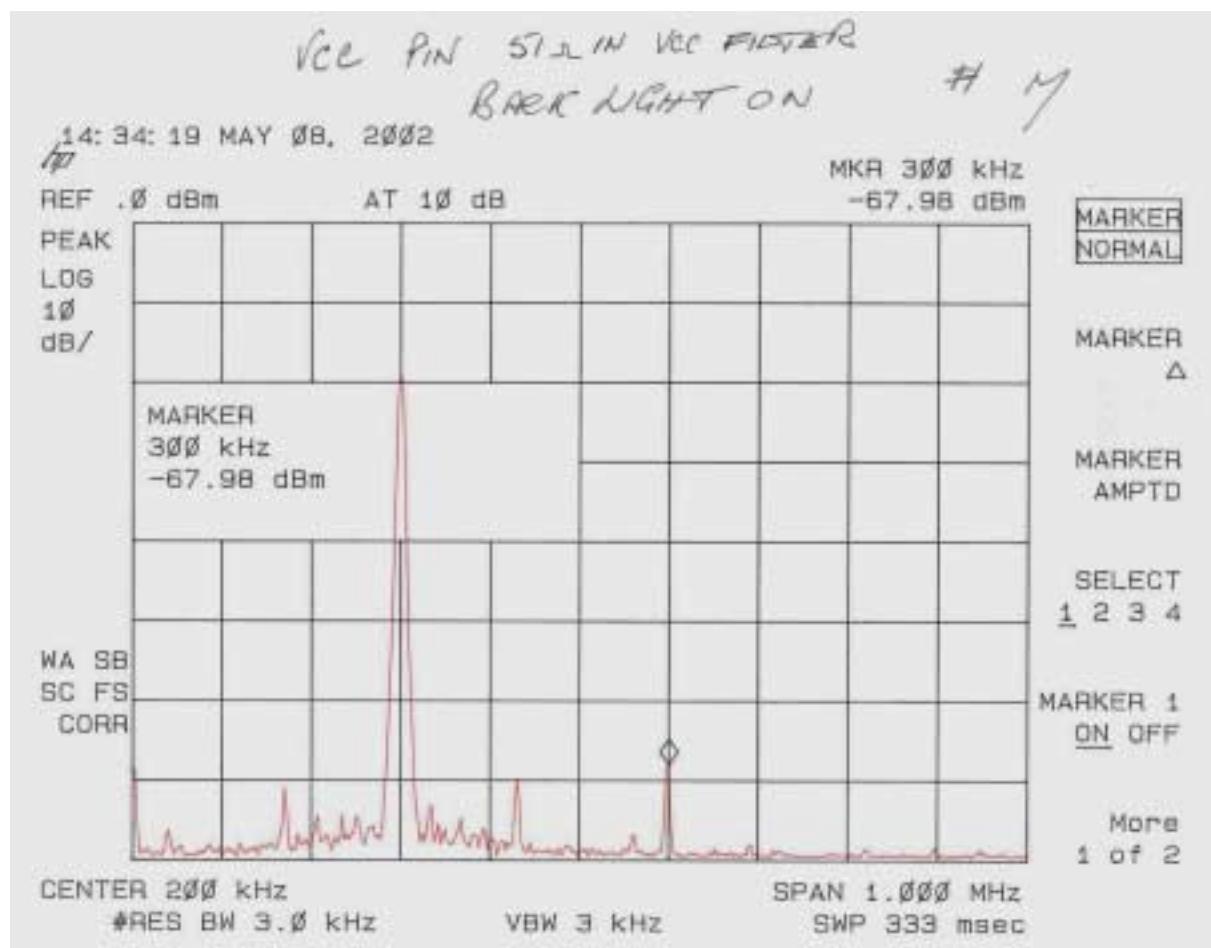


**Figure 3. Board Layouts**



**Graph 1. Spectrum Analyzer Printouts of the VCC Pin to the Module, with Capacitor Decoupling Only, No Series Resistor**

The peaks, which go out to 700 kHz, are generally about the -50 dbm level with a worst-case peak at -48.76 dbm, 2.48 mV peak-to-peak. The second peak, at approximately 120 kHz, is -52dbm, 1.41 mV peak-to-peak. Since the photo diode must be reverse biased from the VCC source, assuming an impedance level of 15K, this represents a peak-to-peak input noise of 165 and 94 nanoamps, respectively. The 300-kHz noise will be rolled off slightly due to the input filter, but the 120-kHz noise will not. One-meter devices with smaller lenses need an IrDA threshold of around 50 nanoamps.



**Graph 2. Spectrum Analyzer Plots of V<sub>CC</sub> Pin with the Addition of a 51-Ohm Resistor Added in the Lead from the Voltage Supply to the V<sub>CC</sub> Pin**

Notice the absence of noise from 300 kHz up and the value of the worst peak at -67.98 dbm. There is a difference of -20 dbm over the case above without a decoupling resistor. This gives an effective input noise (at one frequency) of 16.5 nanoamps; this noise, however, will be rolled off by the input filter by at least 6 dbs.



---

## Information Integrity

The information contained within this document has been verified according to the general principles of electrical and mechanical engineering. Any applicable source code illustrated in the document was either written by an authorized ZiLOG employee or licensed consultant. Permission to use these codes in any form besides the intended application, must be approved through a license agreement between both parties. ZiLOG will not be responsible for any code(s) used beyond the intended application. Contact your local ZiLOG Sales Office to obtain necessary license agreements.

---

## Document Disclaimer

©2002 by ZiLOG, Inc. All rights reserved. Information in this publication concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. ZiLOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZiLOG ALSO DOES NOT ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. Except with the express written approval of ZiLOG, use of information, devices, or technology as critical components of life support systems is not authorized. No licenses are conveyed, implicitly or otherwise, by this document under any intellectual property rights.