

## DETAILED DESCRIPTION

### SPEECH/SOUND QUALITY

ISD's patented ChipCorder technology provides natural record and playback. The ISD1100 series includes devices offered at 5.3 and 6.4 KHz sampling frequencies, allowing the user a choice of speech quality options. The input voice signals are stored directly in nonvolatile EEPROM cells and are reproduced without the synthetic effect often heard with digital solid-state speech solutions. A complete sample is stored in a single cell, minimizing the memory necessary to store a recording of a given duration.

### DURATION

The ISD1100 series devices offers single-chip solutions for 10 and 12 seconds.

### EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

### BASIC OPERATION

The ISD1100 ChipCorder series devices are controlled by a single signal,  $\overline{REC}$ , and either of two push-button control playback signals,  $\overline{PLAYE}$  (edge-activated playback), and  $\overline{PLAYL}$  (level-activated playback). The ISD1100 series parts are configured for simplicity of design in a single-message application. Device operation is explained on page 14.

### AUTOMATIC POWER-DOWN MODE

At the end of a playback or record cycle, the ISD1100 series devices automatically return to a low-power standby mode, consuming typically  $0.5 \mu\text{A}$ . During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after  $\overline{REC}$  is released HIGH.

### LOOPING CAPABILITY

The ISD1100 series devices have a built-in looping function, enabling the continuous repeating of a single message. Looping is initiated by a negative transition on the  $\overline{PLAYE}$  pin with A3 held HIGH.  $\overline{PLAYE}$  is then brought back HIGH. Looping will continue indefinitely with all three control pins ( $\overline{PLAYL}$ ,  $\overline{PLAYE}$ , and  $\overline{REC}$ ) remaining HIGH. Pulsing  $\overline{PLAYL}$  LOW will end the playback.

### ADDRESSING (OPTIONAL)

In addition to providing simple message playback, the ISD1100 series devices provide a full addressing capability.

The ISD1100 series devices have 80 distinct addressable segments providing the following resolution per segment. See Application Information for ISD1100 series devices address tables.

**Table 1: Device Playback/Record Durations**

Part Number	Minimum Duration (Seconds)
ISD1110	125 ms
ISD1112	150 ms

## PIN DESCRIPTIONS

**NOTE** The  $\overline{REC}$  signal is debounced for 50 ms on the rising edge to prevent a false retriggering from a push-button switch.  $\overline{REC}$ ,  $\overline{PLAYL}$ , and  $\overline{PLAYE}$  have internal pullups to  $V_{CC}$ . Holding one of these pins LOW will increase standby current consumption.

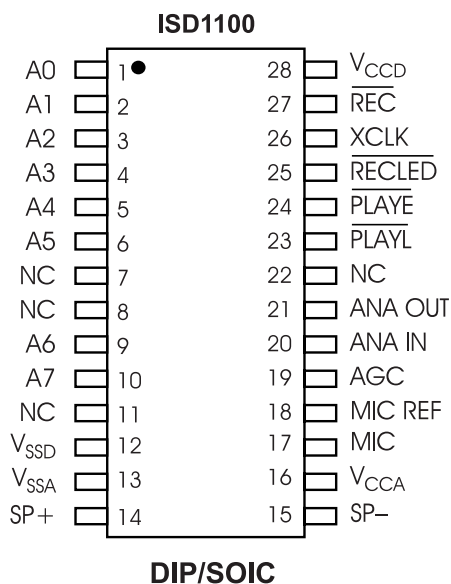
### VOLTAGE INPUTS ( $V_{CCA}$ , $V_{CCD}$ )

Analog and digital circuits internal to the ISD1100 series devices use separate power buses to minimize noise on the chip. These power buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the power supply be decoupled as close as possible to the package.

### GROUND INPUTS ( $V_{SSA}$ , $V_{SSD}$ )

Similar to  $V_{CCA}$  and  $V_{CCD}$ , the analog and digital circuits internal to the ISD1100 series devices use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

Figure 1: ISD1100 Series Pinout



**NOTE:** NC means must Not Connect.

### RECORD ( $\overline{REC}$ )

The  $\overline{REC}$  input is an active-LOW record signal. The device records whenever  $\overline{REC}$  is LOW. This signal must remain LOW for the duration of the recording.  $\overline{REC}$  takes precedence over either playback ( $\overline{PLAYE}$  or  $\overline{PLAYL}$ ) signal. If  $\overline{REC}$  is pulled LOW during a playback cycle, the playback immediately ceases and recording begins.

A record cycle is completed when  $\overline{REC}$  is pulled HIGH. An end-of-message (EOM) marker is internally recorded, enabling a subsequent playback cycle to terminate appropriately. The device automatically powers down to standby mode when  $\overline{REC}$  goes HIGH. This pin has an internal pull-up device.

### PLAYBACK, EDGE-ACTIVATED ( $\overline{PLAYE}$ )

When a LOW-going transition is detected on this input signal, a playback cycle begins. Playback continues until an end-of-message marker is encountered or the end of the memory space is reached. Upon completion of the playback cycle, the device automatically powers down into standby mode. Taking  $\overline{PLAYE}$  HIGH during a playback cycle will not terminate the current cycle. This pin has an internal pull-up device.

### PLAYBACK, LEVEL-ACTIVATED ( $\overline{PLAYL}$ )

When this input signal transitions from HIGH to LOW, a playback cycle is initiated. Playback continues until  $\overline{PLAYL}$  is pulled HIGH, an end-of-message marker is detected, or the end of the device space is reached. The device automatically powers down to standby mode upon completion of the playback cycle. This pin has an internal pull-up device.

**NOTE** In playback, if either  $\overline{PLAYE}$  or  $\overline{PLAYL}$  is held LOW during EOM or OVERFLOW, the device will still enter standby and the internal oscillator and timing generator will stop. However, the rising edge of  $\overline{PLAYE}$  and  $\overline{PLAYL}$  are not debounced, and any subsequent falling edge (particularly switch bounce) present on the input pins will initiate another playback.

### RECORD LED OUTPUT ( $\overline{\text{RECLED}}$ )

The output  $\overline{\text{RECLED}}$  is LOW during a record cycle. It can be used to drive an LED to provide feedback that a record cycle is in progress. In addition,  $\overline{\text{RECLED}}$  pulses LOW momentarily when an end-of-message marker is encountered in a playback cycle.

### MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of the preamplifier from  $-15$  to  $24$  dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal  $10\text{ K}\Omega$  resistance on this pin, determine the low-frequency cutoff for the ISD1100 series passband. See ISD Application Information for additional information on low-frequency cutoff calculations.

### MICROPHONE REFERENCE (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-cancelling, or common-mode rejection, input to the device when connected differentially to a microphone.

### AUTOMATIC GAIN CONTROL (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of sound, from whispers to loud sounds, to be recorded with minimal distortion. The "attack" time is determined by the time constant of a  $5\text{ K}\Omega$  internal resistance and an external capacitor (C6 on Figure 4) connected from the AGC pin to  $V_{\text{SSA}}$  analog ground. The "release" time is determined by the time constant of an external resistor (R5) and an external capacitor (C6) connected in parallel between the AGC pin and  $V_{\text{SSA}}$  analog ground. Nominal values of  $470\text{ K}\Omega$  and  $4.7\text{ }\mu\text{F}$  give satisfactory results in most cases.

### ANALOG OUTPUT (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

### ANALOG INPUT (ANA IN)

The ANA IN pin transfers the input signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the  $3\text{ K}\Omega$  input impedance at ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

### OPTIONAL EXTERNAL CLOCK (XCLK)

The external clock input for the ISD1100 series devices has an internal pull-down resistor. The ISD1100 series is configured at the factory with an internal sampling clock frequency that guarantees its minimal nominal record/playback time. For instance, an ISD1110 operating within specification will always be observed to have a minimum of 10 seconds of recording time. The sampling frequency is maintained to a total variation of  $\pm 2.25$  percent over the commercial temperature and operating voltage ranges while still maintaining the minimum duration specified. This will result in some devices having a few percent more than nominal recording time. If greater precision is required, the device can be clocked through the XCLK pin as follows:

**Table 2: External Clock Sample Rates**

Part Number	Sample Rate	Required Clock
ISD1110	6.4 KHz	819.2 KHz
ISD1112	5.3 KHz	682.7 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. **if the XCLK is not used, this input should be connected to ground.** Please see Application Information for the ISD1100 series for more details on external clocking.

### **SPEAKER OUTPUTS (SP+, SP-)**

The SP+ and SP- pins provide direct drive for loudspeakers with impedances as low as 16  $\Omega$ . A single output may be used, but, for direct-drive loudspeakers, the two opposite-polarity outputs provide an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP- are used, a speaker-coupling capacitor is not required. A single-ended connection will require an AC-coupling capacitor between the SP pin and the speaker. The speaker outputs are in a high-impedance state during a record cycle, and held at  $V_{SSA}$  during power-down.

### **ADDRESS INPUTS (A0–A7)**

The Address Inputs have two functions, depending upon the level of the two Most Significant Bits (MSB) of the address (A6 and A7).

If either of the two MSBs is LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of  $\overline{\text{PLAYE}}$ ,  $\overline{\text{PLAYL}}$  or  $\overline{\text{REC}}$ . A6 and A7 have internal pull-up devices. A0, A1, A2, A3, A4 and A5 have internal pull-down devices. This allows the signals to be left floating if not used. Each of these internal pull-up or pull-down devices have a value of 50K $\Omega$  to 100K $\Omega$ .

### **LOOPING CAPABILITY**

The ISD1100 series device has a built-in looping function enabling it to continuously repeat a single message. This is accomplished by taking A3 HIGH to continuously loop from the end of the message to the beginning of the message space. Looping is initiated by a negative transition on  $\overline{\text{PLAYE}}$  pin with A7, A6 and A3 held HIGH. Then  $\overline{\text{PLAYE}}$  is brought back HIGH. Looping will continue indefinitely with all three control pins ( $\overline{\text{PLAYL}}$ ,  $\overline{\text{PLAYE}}$ ,  $\overline{\text{REC}}$ ) remaining HIGH.

To stop the looping,  $\overline{\text{PLAYL}}$  pin is momentarily taken LOW, then back HIGH. As long as A7, A6 and A3 remain HIGH, a new playback loop will begin with the next negative transition on the  $\overline{\text{PLAYE}}$  pin.

Another way to control looping is to use  $\overline{\text{PLAYL}}$  pin alone. Taking this pin LOW begins the looping and it continues until the pin is taken HIGH again. This is a continuous control rather than the pulsed control of the previous paragraph.

TIMING DIAGRAMS

Figure 2: Record

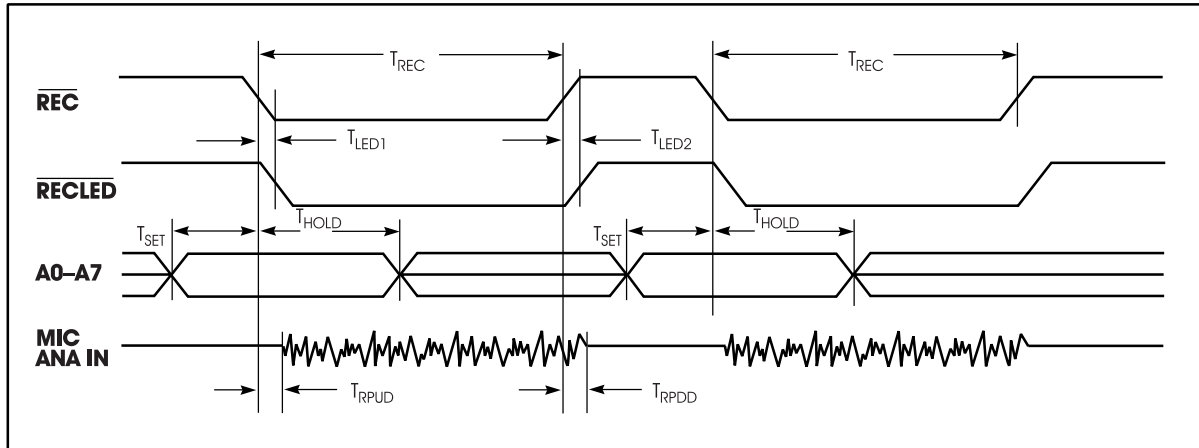
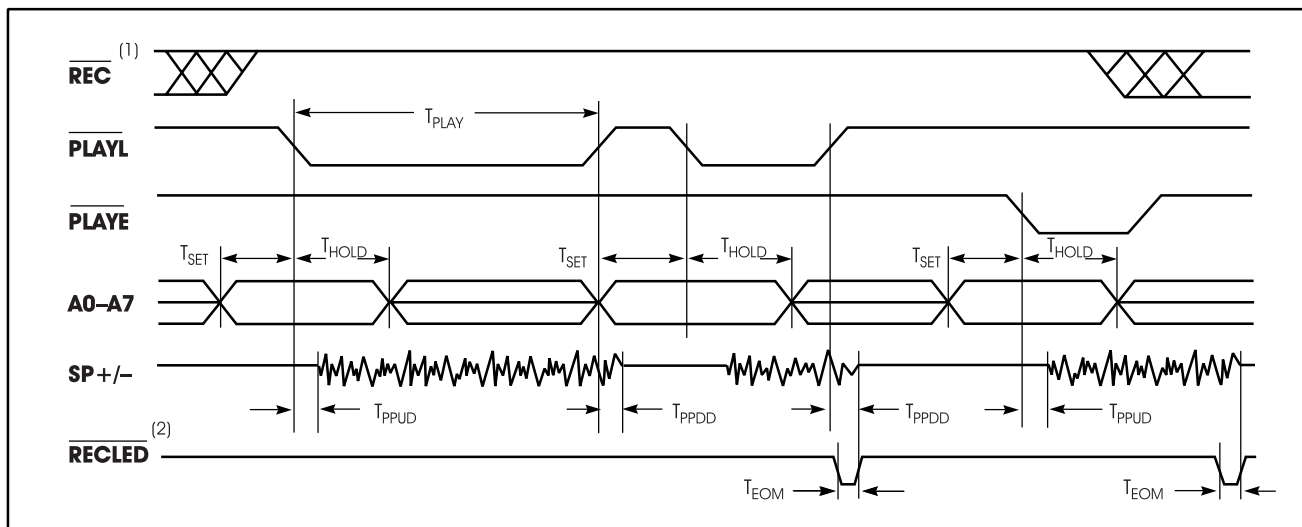


Figure 3: Playback



1.  $\overline{\text{REC}}$  must be HIGH for the entire duration of a playback cycle.
2.  $\overline{\text{RECLEd}}$  functions as an EOM during playback.

**Table 3: Absolute Maximum Ratings**  
(Packaged Parts)<sup>(1)</sup>

Condition	Value
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pin	(V <sub>SS</sub> - 0.3 V) to (V <sub>CC</sub> + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V <sub>SS</sub> - 1.0 V) to (V <sub>CC</sub> + 1.0 V)
Lead temperature (soldering - 10 seconds)	300°C
V <sub>CC</sub> - V <sub>SS</sub>	-0.3V to +7.0 V

**1.** Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

**Table 4: Operating Conditions**  
(Packaged Parts)

Condition	Value
Commercial operating temperature range <sup>(1)</sup>	0°C to +70°C
Supply voltage (V <sub>CC</sub> ) <sup>(2)</sup>	+4.5 V to +5.5 V
Ground voltage (V <sub>SS</sub> ) <sup>(3)</sup>	0 V

- 1.** Case temperature.
- 2.** V<sub>CC</sub> = V<sub>CCA</sub> = V<sub>CCD</sub>.
- 3.** V<sub>SS</sub> = V<sub>SSA</sub> = V<sub>SSD</sub>.

**Table 5: DC Parameters** (Packaged Parts)

Symbol	Parameters	Min <sup>(2)</sup>	Typ <sup>(1)</sup>	Max <sup>(2)</sup>	Units	Conditions
V <sub>IL</sub>	Input Low Voltage			0.8	V	
V <sub>IH</sub>	Input High Voltage	2.4			V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 4.0 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -1.6 mA
I <sub>CC</sub>	V <sub>CC</sub> Current (Operating)		15	30	mA	V <sub>CC</sub> = 5.5 V <sup>(3)</sup> , R <sub>EXT</sub> = ∞
I <sub>SB</sub>	V <sub>CC</sub> Current (Standby)		0.5	2	μA	<sup>(3)</sup> <sup>(4)</sup>
I <sub>IL</sub>	Input Leakage Current			±1	μA	
I <sub>ILPU</sub>	Input Current LOW w/Pull Up			-130	μA	Force V <sub>SS</sub> <sup>(5)</sup>
I <sub>ILPD</sub>	Input Current HIGH w/Pull Down			130	μA	Force V <sub>CC</sub> <sup>(6)</sup>
R <sub>EXT</sub>	Output Load Impedance	16			Ω	Speaker Load
R <sub>MIC</sub>	Preamplifier Input Resistance		10		KΩ	Pins 17, 18
R <sub>ANA IN</sub>	ANA IN Input Resistance		3		KΩ	
A <sub>PRE1</sub>	Preamplifier Gain 1		24		dB	AGC = 0.0 V

Table 5: DC Parameters (Packaged Parts)

Symbol	Parameters	Min <sup>(2)</sup>	Typ <sup>(1)</sup>	Max <sup>(2)</sup>	Units	Conditions
A <sub>PRE2</sub>	Preamplifier Gain 2		-45	-15	dB	AGC = 2.5 V
A <sub>ARP</sub>	ANA IN to SP +/- Gain		22		dB	
R <sub>AGC</sub>	AGC Output Resistance		5		kΩ	
I <sub>PREH</sub>	Preamplifier Out Source		-2		mA	@ V <sub>OUT</sub> = 1.0 V
I <sub>PREL</sub>	Preamplifier In Sink		0.5		mA	@ V <sub>OUT</sub> = 2.0 V

1. Typical values @ T<sub>A</sub> = 25°C and 5.0 V.
2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
3. V<sub>CCA</sub> and V<sub>CCD</sub> connected together.
4. REC, PLAYL, and PLAYE must be at V<sub>CCD</sub>.
5. REC, PLAYL, and PLAYE, A6, A7.
6. A0–A5, XCLK.

Table 6: AC Parameters (Packaged Parts)

Symbol	Characteristic	Min <sup>(2)</sup>	Typ <sup>(1)</sup>	Max <sup>(2)</sup>	Units	Conditions	
F <sub>S</sub>	Sampling Frequency	ISD1110		6.4	KHz	<sup>(5)</sup>	
		ISD1112		5.3	KHz	<sup>(5)</sup>	
F <sub>CF</sub>	Filter Pass Band	ISD1110	2.6		KHz	3 dB Roll-Off Point <sup>(3)(6)</sup>	
		ISD1112	2.2		KHz	3 dB Roll-Off Point <sup>(3)(6)</sup>	
T <sub>REC</sub>	Record Duration	ISD1110	10		sec		
		ISD1112	12		sec		
T <sub>PLAY</sub>	Playback Duration	ISD1110	10		sec	<sup>(5)</sup>	
		ISD1112	12		sec	<sup>(5)</sup>	
T <sub>LED1</sub>	<u>RECLED</u> ON Delay		5		μsec		
T <sub>LED2</sub>	<u>RECLED</u> OFF Delay	ISD1110	40	48.5	100	msec	
		ISD1112	50	58.3	105	msec	
T <sub>SET</sub>	A0–A7 Setup Time		300		nsec		
T <sub>HOLD</sub>	A0–A7 Hold Time		0		nsec		
T <sub>RPUD</sub>	Record Power-Up Delay	ISD1110		32		msec	
		ISD1112		39		msec	
T <sub>RPDD</sub>	Record Power-Down Delay	ISD1110		32		msec	
		ISD1112		39		msec	
T <sub>PPUD</sub>	Play Power-Up Delay	ISD1110		32		msec	
		ISD1112		39		msec	
T <sub>PPDD</sub>	Play Power-Down Delay	ISD1110		8.1		msec	
		ISD1112		9.7		msec	

Table 6: AC Parameters (Packaged Parts)

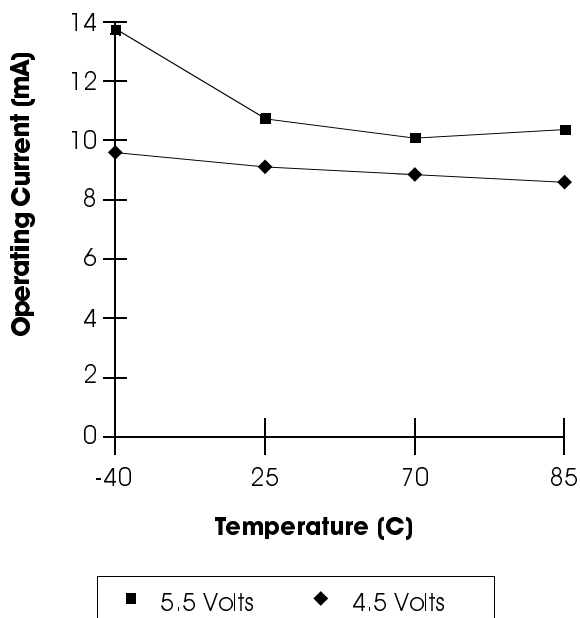
Symbol	Characteristic	Min <sup>(2)</sup>	Typ <sup>(1)</sup>	Max <sup>(2)</sup>	Units	Conditions
T <sub>EOM</sub>	EOM Pulse Width		ISD1110	15.62		msec
			ISD1112	5		
THD	Total Harmonic Distortion		1		%	@ 1 KHz
P <sub>OUT</sub>	Speaker Output Power		12.2		mW	R <sub>EXT</sub> = 16 Ω
V <sub>OUT</sub>	Voltage Across Speaker Pins		1.25	2.5	MVp-p	R <sub>EXT</sub> = 600 Ω
V <sub>IN1</sub>	MIC Input Voltage			20	mV	Peak-to-Peak <sup>(4)</sup>
V <sub>IN2</sub>	ANA IN Input Voltage			50	mV	Peak-to-Peak

1. Typical values @ T<sub>A</sub> = 25°C and 5.0 V.
2. All Min/Max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.
3. Low-frequency cutoff depends upon value of external capacitors (see Pin Descriptions).
4. With 5.1 KΩ series resistor at ANA IN.
5. Sampling frequency and playback duration will vary as much as ±2.25 percent over the commercial temperature and voltage ranges. All devices will meet the maximum sampling frequency and minimum playback duration parameters. For greater stability, an external clock can be utilized (see Pin Descriptions).
6. Filter specification applies to the antialiasing filter and the smoothing filter.

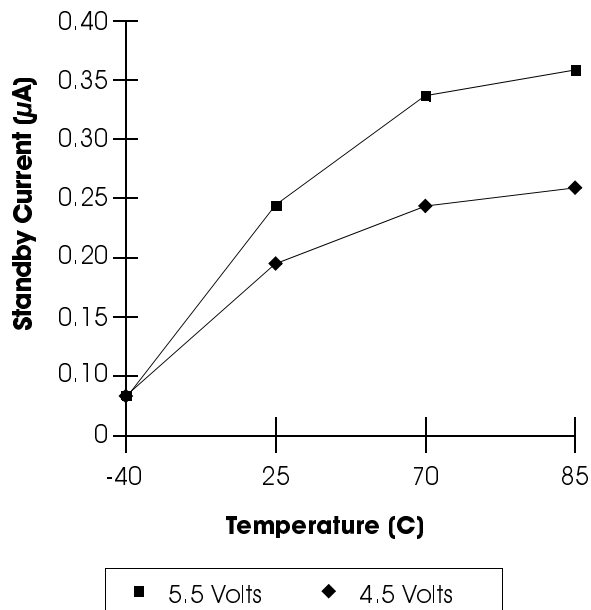


**TYPICAL PARAMETER VARIATION WITH VOLTAGE AND TEMPERATURE (PACKAGED PARTS)**

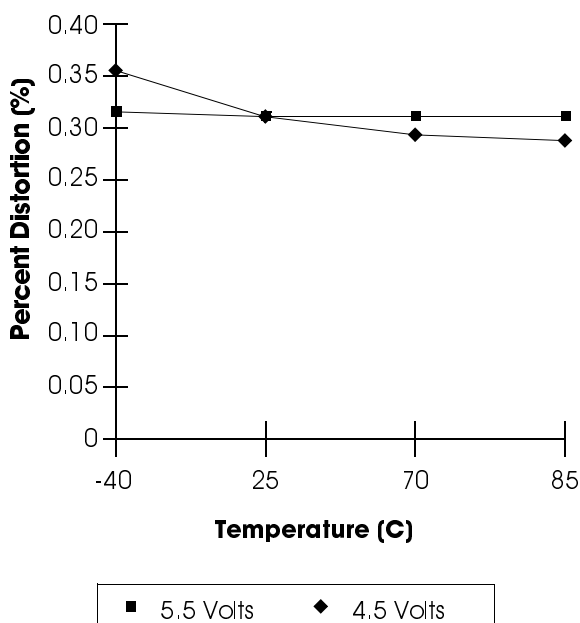
**Chart 1: Record Mode Operating Current ( $I_{CC}$ )**



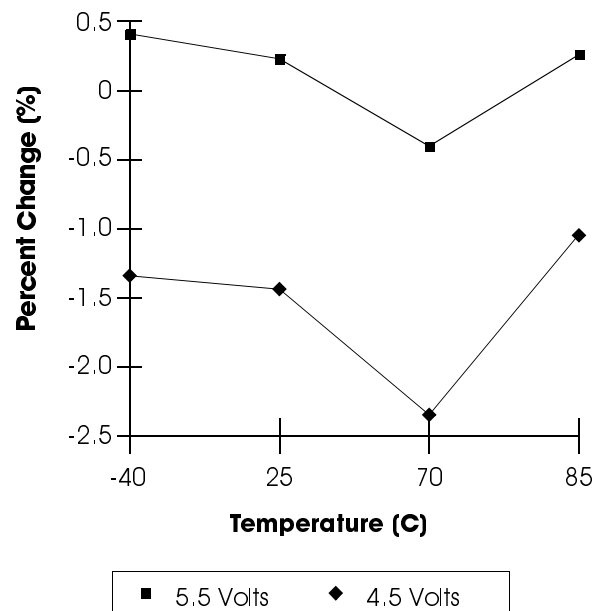
**Chart 3: Standby Current ( $I_{SB}$ )**



**Chart 2: Total Harmonic Distortion**



**Chart 4: Oscillator Stability**



**Table 7: Absolute Maximum Ratings (Die)<sup>(1)</sup>**

Condition	Value
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to any pad	(V <sub>SS</sub> - 0.3 V) to (V <sub>CC</sub> + 0.3 V)
Voltage applied to any pad (Input current limited to ±20 mA)	(V <sub>SS</sub> - 1.0 V) to (V <sub>CC</sub> + 1.0 V)
V <sub>CC</sub> - V <sub>SS</sub>	-0.3 V to +7.0 V

1. Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.

**Table 8: Operating Conditions (Die)**

Condition	Value
Operating temperature range	0°C to +50°C
Supply voltage (V <sub>CC</sub> ) <sup>(1)</sup>	+4.5 V to +6.5 V
Ground voltage (V <sub>SS</sub> ) <sup>(2)</sup>	0 V

1. V<sub>CC</sub> = V<sub>CCA</sub> = V<sub>CCD</sub>.

2. V<sub>SS</sub> = V<sub>SSA</sub> = V<sub>SSD</sub>.

**Table 9: DC Parameters (Die)**

Symbol	Parameters	Min <sup>(2)</sup>	Typ <sup>(1)</sup>	Max <sup>(2)</sup>	Units	Conditions
V <sub>IL</sub>	Input Low Voltage			0.8	V	
V <sub>IH</sub>	Input High Voltage	2.4			V	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 4.0 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -1.6 mA
I <sub>CC</sub>	V <sub>CC</sub> Current (Operating)		15	30	mA	V <sub>CC</sub> = 5.5 V <sup>(3)</sup> , R <sub>EXT</sub> = ∞
I <sub>SB</sub>	V <sub>CC</sub> Current (Standby)		0.5	2	μA	<sup>(3)</sup> <sup>(4)</sup>
I <sub>IL</sub>	Input Leakage Current			±1	μA	
I <sub>LPU</sub>	Input Current LOW w/Pull Up			-130	μA	Force V <sub>SS</sub> <sup>(5)</sup>
I <sub>LDP</sub>	Input Current HIGH w/Pull Down			130	μA	Force V <sub>CC</sub> <sup>(6)</sup>
R <sub>EXT</sub>	Output Load Impedance	16			Ω	Speaker Load
R <sub>MIC</sub>	Preamp In Input Resistance		10		KΩ	Pins 17, 18
R <sub>ANA IN</sub>	ANA IN Input Resistance		3		KΩ	
A <sub>PRE1</sub>	Preamp Gain 1		24		dB	AGC = 0.0 V
A <sub>PRE2</sub>	Preamp Gain 2		-45	-15	dB	AGC = 2.5 V